MD KAWSER BEPARY

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Professional Summary

Ph.D. candidate specializing in SoC/ASIC design, digital hardware verification, and side-channel analysis, with strong proficiency in SystemVerilog, formal methods, and automated CAD flows. Skilled in RTL coding, embedded applications, hardware security verification, and performance/power optimization, delivering robust, high-performance silicon solutions.

Education

- **University of Florida** — Gainesville, FL
  Doctor of Philosophy (Ph.D.) in Electrical and Computer Engineering — *Jan 2021 - Aug 2025 (Expected)*
  Advisor: Prof. Mark Tehranipoor — *CGPA: **3.95/4.00***

- **The University of Alabama in Huntsville** — Huntsville, AL
  Master of Science (M.Sc.) in Computer Engineering — *Aug 2019 - Dec 2020*
  Advisor: Prof. M. Tauhidur Rahman — *CGPA: **3.71/4.00***

- **Bangladesh University of Engineering and Technology (BUET)** — Dhaka, Bangladesh
  Bachelor of Science (B.Sc.) in Electrical and Electronic Engineering — *Jul 2014 - Oct 2018*
  *CGPA: **3.51/4.00***

Technical Skills

- **Programming Languages**: Python, C/C++, Rust, Verilog, VHDL, SystemVerilog, Assembly (RISC-V/MIPS)
- **Verification & EDA Tools**:
  - **RTL Design & Synthesis**: Synopsys Design Compiler, Xilinx Vivado, Cadence Genus, ABC
  - **Functional Verification**: ModelSim, Synopsys VCS, SimVision, SystemVerilog Assertions (SVA), UVM
  - **Formal Verification**: Cadence JasperGold, Synopsys Formality
  - **Physical Design**: Cadence Innovus, Virtuoso, Synopsys ICC2
  - **Other EDA Tools**: Synopsys PrimeTime, TetraMax, StarRC
- **Scripting**: Tcl, Unix Shell, GNU Make, CMake
- **Data Analysis & Machine Learning**: Scikit-learn, TensorFlow, Keras, PyTorch
- **Other Software and Tools**: Linux, Git, PAPI, Perforce, LaTeX

Experience

- **Synopsys Inc.** — Sunnyvale, CA
  Graduate Technical Intern (Security IP Team), Solutions Group — *May 2023 - Dec 2023*
  - Developed embedded applications for secure boot, TLS communication, and cryptographic services under DARPA-funded AISS (Automatic Implementation of Secure Silicon) project.
  - Implemented ASCON lightweight cryptographic protocols for embedded firmware security, including encryption and authentication mechanisms.
  - Integrated ASCON authenticated encryption and hashing hardware module to the Synopsys security engine subsystem; implemented a masking scheme for side-channel resiliency.

- **Florida Institute for Cybersecurity (FICS) Research, University of Florida** — Gainesville, FL
  Graduate Research Assistant — *Jan 2021 - Current*
  - Developing machine learning-based side-channel leakage modeling framework at pre-silicon stage, enhancing the security of cryptographic designs against physical attacks.
  - Created an EM-based side-channel disassembler to reconstruct executed microcontroller instructions, enabling robust analysis in secure embedded systems.
  - Devised a PMU-based approach for detecting cpu workloads and mitigating cache side-channel vulnerabilities to counter speculative execution attacks.
  - Implemented an automated CAD toolflow to evaluate physical-design aware EM side-channel vulnerability at gate-level, enabling fast security sign-off at pre-silicon.
  - Built a Python-based framework to estimate IP/SoC power side-channel resiliency at RTL for a DARPA-funded AISS project, providing actionable metrics in collaboration with Synopsys.

- **Department of ECE, University of Florida** Gainesville, FL
  Graduate Teaching Assistant - Intro to Hardware Security and Trust *Aug 2022 - Dec 2022*
  - Designed hands-on tutorials for industry-standard EDA tools, assisting students in VLSI synthesis, functional verification, and security analysis.
  - Managed grading, projects, and exam evaluations while providing mentorship to students on security verification methodologies.
- **Department of ECE, The University of Alabama in Huntsville** Huntsville, AL
  Graduate Research Assistant *Aug 2019 - Dec 2020*
  - Developed C++ scripts to interface commercial DDR3 DRAM chips deployed on an FPGA board to execute read/write operations with configurable timing parameters.
  - Conducted stress testing and bit-flip analysis on DRAM modules to evaluate security vulnerabilities and reliability issues.
- **Department of ECE, The University of Alabama in Huntsville** Huntsville, AL
  Graduate Teaching Assistant - Computer Organization, Intro to Computer Architecture *Aug 2020 - Dec 2020*
  - Assisted 100+ graduate/undergraduate students with grading homework, quizzes, projects, and exams on concepts of computer organization, architecture, memory hierarchy, assembly language, and MIPS ISA.

Publications

- **MK Bepary**, T Zhang, J Zhou, et al., "Towards Efficient Gate-Level Electromagnetic Side-Channel Leakage Modeling and Vulnerability Assessment," Journal of Hardware and Systems Security, 2025. (link)
- **MK Bepary**, T Zhang, F Farahmandi and M Tehranipoor. "PreSCAN: A Comprehensive Review of Pre-Silicon Physical Side-Channel Vulnerability Assessment Methodologies." Chips 3, no. 3 (2024). (link)
- T Rahman, **MK Bepary**, MSUl Haque, M Tehranipoor and F Rahman, "Design and Security-Mitigation of Custom and Configurable Hardware Cryptosystems," 2023 IEEE 16th Dallas Circuits and Systems Conference (DCAS), Denton, TX, USA, 2023, pp. 1-6. (link)
- **MK Bepary**, F Rahman, F Farahmandi, and M Tehranipoor. "Security Assessment and Modeling of EM Side-channel Leakage at Gate-Level." in Annual GOMACTech Workshop 2023, USA.
- B Ahmed, **MK Bepary**, N Pundir, M Borza, et al. "Quantifiable Assurance: From IPs to Platforms." Cryptology ePrint Archive (2021). (link)
- **MK Bepary**, BMSB Talukder, and MT Rahman. "DRAM Retention Behavior with Accelerated Aging in Commercial Chips." Applied Sciences 12, no. 9 (2022): 4332. (link)

Relevant Coursework

- **Computer Engineering**: Computer Architecture, System-on-Chip Design, Reconfigurable Computing, VLSI HDL/ Modeling, Advanced Computer Architecture, Parallel Programming, Advanced VLSI
- **Hardware Security**: Cybersecurity Engineering, Hardware Security and Trust, CAD for Hardware Security Verification, Advanced Hardware Security
- **Machine Learning**: Data Mining, Intro to Machine Learning, Probability and Statistics

Selected Academic Projects

- **System-on-Chip (SoC) Design**: Implemented a SoC hardware design using MicroBlaze processor, peripheral IP integration (AXI, APB), bus protocol (APB), and developed baremetal C applications (2023).
- **Convolution and DRAM DMA on FPGA**: Created a custom hardware implementation of 1-D Time-Domain Convolution operation and DRAM DMA interface on Zedboard to improve performance using parallelism (2024).
- **Property-based security verification of an RSA controller**: Used SystemVerilog Assertions in Cadence Jasper to verify security properties of an RSA module (2022).
- **Implementation of FPGA Pong Game**: Built the VGA controller and Pong Game controller on a Xilinx FPGA using a MicroBlaze processor and I/O peripherals (2023).
- **Performance analysis of cache replacement policies**: Implemented different cache replacement policies (LRU, pseudo-LRU, FIFO, random, MRU, LFU, etc.) on x86 architecture using Gem-5 to analyze the performance improvement on benchmark programs (2020).
- **Deep-learning based hand-written character recognition**: Developed a CNN pipeline in Python (Keras, scikit-learn) to classify hand-written characters, achieving 98% accuracy (2022) (github).

Honors and Awards

- 1st Place in 2022 IEEE HOST Microelectronics Security Challenge (github), Undergrad Dean's List (2015), Education Board Merit Scholarship (Secondary and Higher Secondary).